

## 17.6 A Single-Chip Quad-Band GSM/GPRS Transceiver in 0.18 $\mu$ m Standard CMOS

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CMOS RF has evolved from a novelty to a necessity with the merger of all analog and digital functionality into a single chip for standards such as Bluetooth and WLAN/802.11. The stringent performance requirements associated with cellular standards such as GSM, however, has either limited the level of RF transceiver integration, or compelled the use of alternative technologies such as BiCMOS or bipolar [1]. In this paper, a fully integrated quad-band GSM/GPRS transceiver, fabricated in a 0.18 $\mu$ m CMOS process, is described. This device integrates all the RF and analog transceiver functionality in a single-silicon substrate while meeting the performance requirements of the GSM standard. The challenges of CMOS technology are overcome by careful architectural decisions, appropriate circuit-design techniques, and self-calibrated analog circuits. Wherever possible, the availability of high-density CMOS logic is exploited by pushing the design complexity into the digital domain.

Figure 17.6.1 shows the block diagram of the transceiver IC and the necessary external RF components. Only a switchplexer, a power amplifier module, input SAW filters, and matching components are needed to complete the RF front-end. All the VCOs, TX and RX signal path filters, and PLLs are integrated.

The receiver uses a low-IF architecture. Compared to zero IF, this architecture is more tolerant to impairments due to  $1/f$  noise, DC offsets, and finite receiver IIP2. The LNAs are implemented as fully differential common-source amplifiers with on-chip inductive degeneration for impedance matching and gain peaking. The LNAs also implement a low-gain mode. Following the LNAs, quadrature mixers down-convert the desired RF signal to a low IF. The low-IF section of the receiver consists of a 5<sup>th</sup>-order complex Butterworth filter and PGA. This is formed by cascading five complex pole stages, each implemented as shown in Fig. 17.6.2 [2]. Using a 26MHz crystal as a reference, an on-chip tuning circuit estimates the RC time constant on the transceiver. The capacitor array  $C_2$  is then programmed to correct for process- and temperature-related variations in the filter frequency response. Each complex filter stage contributes to the rejection of the GSM blockers and the image signal, and provides programmable amplification of the desired signal. The gain distribution and the sequencing of the filter poles are selected to maximize the overall RX SNR. This programmable-gain IF filter, combined with the LNA gain step, incorporates 100dB of gain programmability. A DC-offset calibration (DCOC) circuit is used to prevent the IF gain stages from saturating. Resistive cross-coupling between the I and Q channels of the filter cause the DC offsets on the I channel to influence the Q channel and vice versa. In order to keep the DCOC loops independent from each other, the DC offset is measured and corrected as shown in Fig. 17.6.2. Following the complex filter, a low-IF demodulation circuit down-converts the IF I and Q signals to baseband frequencies using a digitally synthesized clock.

The transmitter architecture is based on an offset-frequency phase-locked loop (OPLL) [3]. This OPLL includes a quadrature modulator and a fully integrated, low-phase noise RF VCO with an on-chip LC tank (Fig. 17.6.1). Baseband I and Q GMSK signals

are frequency translated to an IF by the quadrature modulator. A 5<sup>th</sup>-order Gm-C low-pass filter eliminates unwanted frequency components. The PFD output is filtered by an on-chip loop filter and is used to drive an RF VCO that covers the GSM-850, GSM-900, DCS-1800 and PCS-1900 bands. Figure 17.6.3 shows the measured TX modulation spectrum and rms phase error for the highest channel of GSM-900 and PCS.

The VCO output drives an on-chip transmit buffer, shown in Fig. 17.6.4. The RF output level from this buffer is programmable to accommodate different PA modules. Single-ended outputs eliminate the need for external baluns. TX output noise in the receive band, one of the most stringent specifications for a GSM transmitter, is determined by a combination of the on-chip VCO phase noise and the TX pre-PA driver noise. To minimize the noise addition and DC current consumption simultaneously, a rail-to-rail signal swing is preserved from the VCO output to the pre-PA driver input. The measured phase noise of the modulated signal at 20MHz frequency offset is -165dBc/Hz for GSM-850 and GSM-900 bands and -162dBc/Hz for DCS and PCS bands. The transmitter architecture and implementation eliminate the need for all external pre- or post-PA transmit band-pass filters and, hence, improve transmitter power efficiency [4].

The time-division duplex nature of GSM is exploited by using a single frequency synthesizer to generate the LO signals for both the transmitter and receiver. A 3<sup>rd</sup>-order  $\Delta\Sigma$  fractional-N synthesizer is used to provide maximum flexibility for the TX and RX mode frequency plans. In the receive mode, the PLL phase noise at 3MHz offset is lower than -141dBc/Hz to meet the blocker requirements for GSM-850 and GSM-900 bands. A VCO with an on-chip inductor is used to meet both RX and TX phase noise requirements with adequate margin.

The settling time of the PLL, critical for GPRS operation, is improved by coarse tuning the VCO using the pre-charge circuit depicted in Fig. 17.6.5. During the pre-charge phase, switch  $pc$  is closed and the  $\bar{pc}$  switches are open. A class-AB driver charges capacitor  $C_2$  to the mid-control voltage in less than 6 $\mu$ s. During normal operation, the driver output is in a high-impedance state, eliminating the need for a series switch in the high-current output path. The transistor  $M_z$  implements the zero-canceling resistor in the active state, and disconnects the compensation capacitor from the output in the high-impedance state. The measured settling time of <160 $\mu$ s meets the GPRS class-12 requirements.

The key RX and TX performance results are listed in Fig. 17.6.6. When integrated into a complete cellular platform with a baseband DSP, a receiver sensitivity of -110dBm is achieved. Figure 17.6.7 shows the die micrograph of the transceiver IC. The chip is fabricated in a 0.18 $\mu$ m CMOS process; it dissipates 93mA in RX mode and 108mA in TX mode.

### Acknowledgements:

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### References:

- [1] E. Duvivier et al., "A Fully Integrated Zero-IF Transceiver for GSM-GPRS Quad Band Application," *ISSCC Dig. Tech. Papers*, pp. 274-275, Feb., 2003.
- [2] J. Crols et al., "Low-IF Topologies for High-Performance Analog Front Ends of Fully Integrated Receivers," *IEEE TCAS-II*, vol. 45, pp. 269-282, March, 1998.
- [3] T. Yamawaki et al., "A 2.7-V GSM RF Transceiver IC," *IEEE J. Solid-State Circuits*, pp. 2089-2096, Dec., 1997.
- [4] J. Tham et al., "A 2.7-V 900-MHz/1.9-GHz Dual-Band Transceiver IC for Digital Wireless Communication," *IEEE J. Solid-State Circuits*, pp. 286-291, March, 1999.

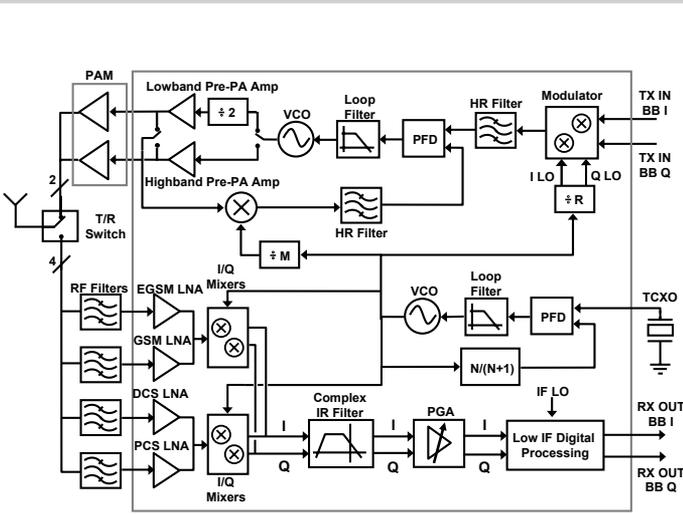


Figure 17.6.1: Quad-band transceiver block diagram.

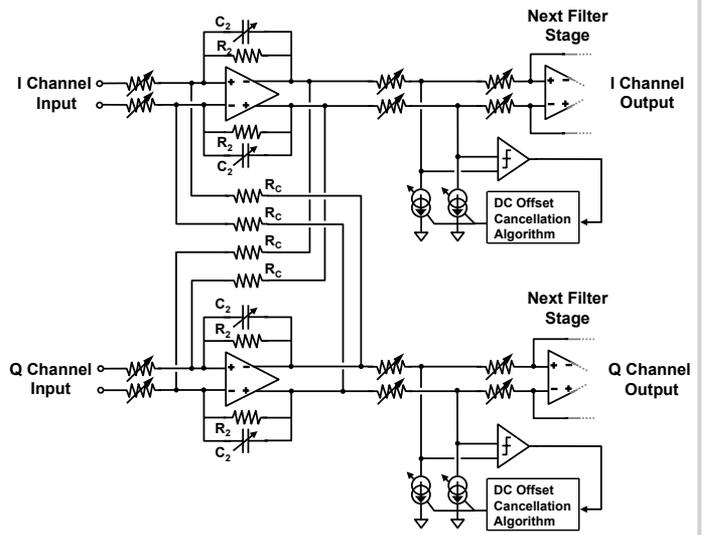


Figure 17.6.2: One complex pole stage of 5<sup>th</sup>-order filter.

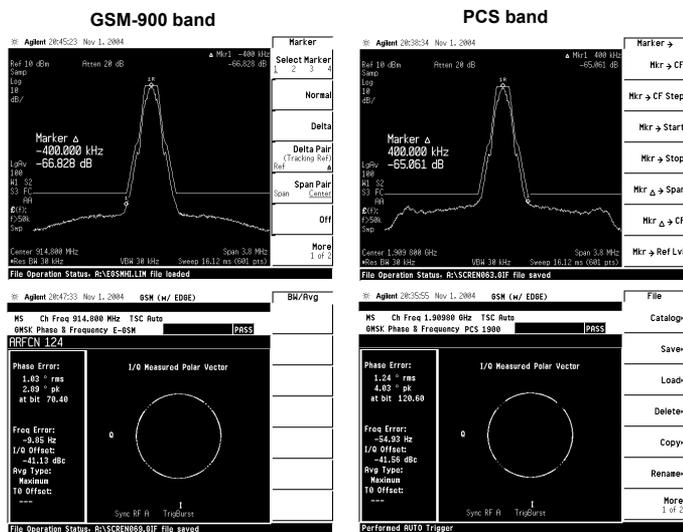


Figure 17.6.3: TX rms phase error and modulation mask.

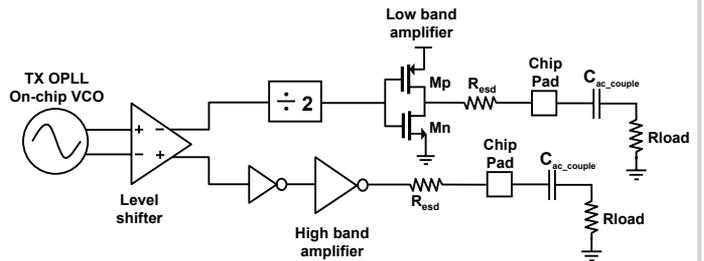


Figure 17.6.4: High and low band pre-PA drivers.

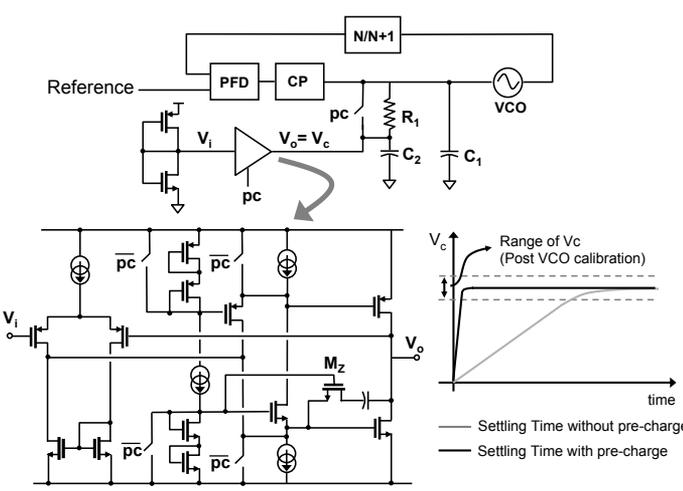


Figure 17.6.5: Fractional-N synthesizer with pre-charger.

Parameter	GSM850/GSM900	DCS1800/PCS1900
Technology	0.18μm CMOS	
Power supply (V)	2.7 to 3.0	
<b>Receiver Measurements</b>		
Noise figure (dB)	2.7	2.7
Input IP3 (dBm)	-15	-15
Input IP2 (dBm)	40	40
RX gain (dB)	100	100
Sensitivity at antenna (dBm)	-110	-109
RX current (mA)	93	95
<b>Transmitter Measurements</b>		
TX RMS phase error (degrees)	1.0	1.2
Output modulation spectrum at 400kHz offset (dBc)	-66	-65
TX noise at 20MHz offset (dBc/Hz)	-165	-162
Worst case PLL settling time (μs)	160	160
TX output power (dBm)	+6	+6
TX Carrier Suppression (dBc)	40	40
TX Sideband Suppression (dBc)	45	45
TX current (mA)	108	112

Figure 17.6.6: Performance summary.

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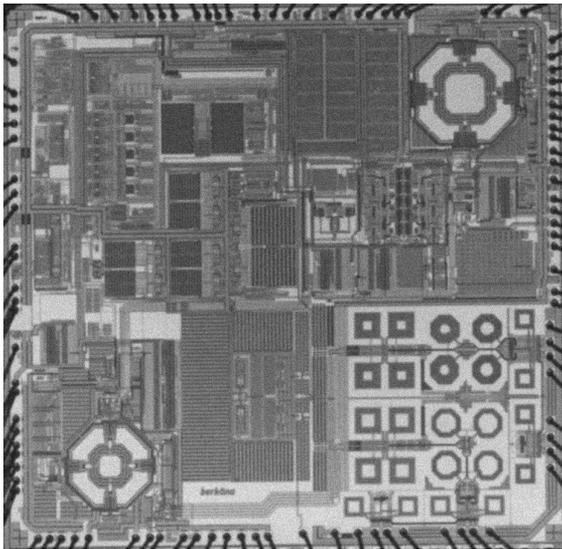


Figure 17.6.7: Single chip quad-band transceiver die micrograph.